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OFFICIAL

Docket No.: YOR91995137X
(20140-00235-US1)
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Panayotis C. Andricacos et al.

Application No.: 10/773,434

Confirmation No.: Not Yet Assigned

Filed: February 9, 2004

Art Unit: Not Yet Assigned

For: ELECTROPLATED INTERCONNECTION
STRUCTURES ON INTEGRATED CIRCUIT
CHIPS

Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits as far as is known to the undersigned (37 CFR 1.97(b)(3)).

Those patent(s) or publication(s) which are marked with a double asterisk (**) next to the Cite No. in the attached form PTO/SB/08 (facsimile) are not supplied because they were previously cited by or submitted to the Office in a prior application number 09/348,632, filed July 6, 1999 and relied upon in this application for an earlier filing date under 35 U.S.C. 120.

Application No.: 10/773,434

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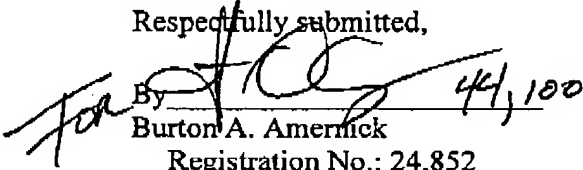
In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0510, under Order No. 20140-00235-US1. A duplicate copy of this paper is enclosed.

Dated: 12 May 2004

Respectfully submitted,

By  44,100
Burton A. Amernick

Registration No.: 24,852
CONNOLLY BOVE LODGE & HUTZ LLP
1990 M Street, N.W., Suite 800
Washington, DC 20036-3425
(202) 331-7111
(202) 293-6229 (Fax)
Attorney for Applicant

PTO/SB/08a/b (05-03)

Approved for use through 07/31/2003. OMB 0851-0031

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Substitute for form 1449A/B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/773,434
				Filing Date	February 9, 2004
				First Named Inventor	Panayotis C. Andricacos
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	2	of	2	Attorney Docket Number	20140-00235-US1

	CE**	Hirano, Makato et al., "Three Dimensional Passive Elements for Compact GaAs MMICs, IEICE Transactions on Electronics, vol. E76-C, No. 6, June 1993, pp. 961-967.	
	CF**	Contolini et al, "Electrochemical Planarization for Multilevel Metallization", J. Electrochem. Soc., vol. 141, No. 9, Sep. 1994, pp 2503-2510.	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. **CITE NO.: Those patent(s) or publication(s) which are marked with an double asterisk (**) next to the Cite No. are not supplied because they were previously cited by or submitted to the Office in a prior application relied upon in this application for an earlier filing date under 35 U.S.C. 120.

¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature		Date Considered	
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